A Fully Integrated CMOS Frequency Synthesizer for Bluetooth

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***Abstract:* — A low power, fully integrated 2.4GHz fractional-N frequency synthesizer for Bluetooth in a 0.25µm CMOS technology is presented. The complete synthesizer, including a fully integrated VCO, consumes 22mA from a 2.5V supply. The integrated VCO reaches a phase noise of -133dBc/Hz at 3MHz. The synthesizer is designed for a direct ΣΔ-modulation of the PLL.**

I. Introduction

The Bluetooth communication standard is becoming more and more important for short-range wireless communication. As it will be more widely used in computers, PDAs, cell phones and other electronic portable devices, the most important goal in developing Bluetooth-solutions will be to reduce the costs and power consumption to a minimum.

The presented chip provides a complete fractional-N frequency synthesizer, designed for the Bluetooth wireless communication standard (Fig. 1). It contains a phase-frequency-detector, a tri-state-chargepump, a fully integrated voltage controlled oscillator (VCO), a multi-modulus-divider and a RF output-buffer, which provides an output power of 0dBm.

By using a fully integrated VCO, the presented transmitter solution increases the level of integration significantly, with a reasonable power consumption that is lower than in most recent transmitter solutions and other direct modulation phase-locked loops (PLL) [1]. The high level of integration minimizes the number of external components, which reduces the production costs compared to conventional transmitter solutions significantly. Only the passive 3rd-order loop filter is located off-chip to reach more flexibility for the prototype. This work is a further step to reach the goal of a low power, low cost Bluetooth solution. The complete chip, excluding the RF-buffer, consumes 22mA from a 2.5V supply. The RF output-buffer draws 12mA.

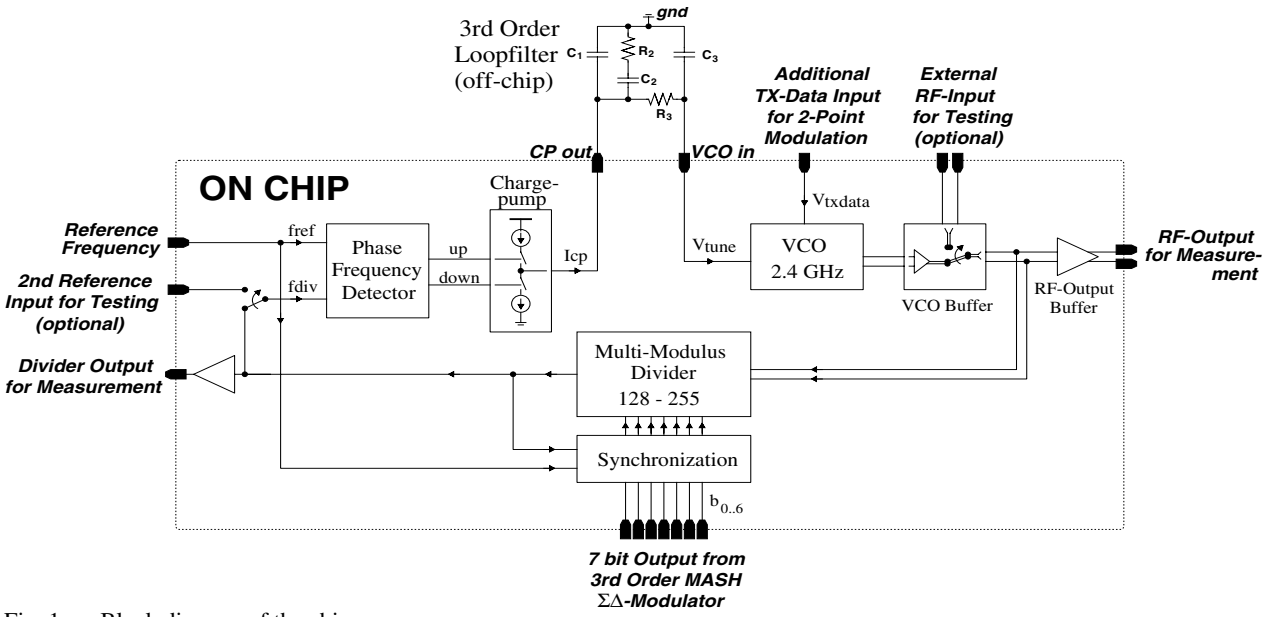

Fig. 1. Block diagram of the chip.

This fractional-N-frequency synthesizer, which provides due to the high reference frequency of 13MHz a fast settling time, is designed for a direct ΣΔ-modulation of the PLL. In a next design step a 3rd-order MASH ΣΔ-modulator will be integrated on the same die to reduce the coupling between the digital and analog parts.

II. Implementation

A. Chargepump

The chargepump (Fig. 2) works with a reference current Iref of 100µA. In this prototype, the current is generated by an external current source. This allows the chargepump current to be changed easily, and thus the open-loop gain, to be more flexible. The mirror factor in the chargepump is 1:4 such that the chargepump provides a current Icp of $\pm$ 400µA.

To achieve a high voltage output range at the chargepump the transistor sizes of the current-mirror transistors (T_1-T_{11}) must be chosen carefully. Also an accurate layout of the chargepump is important to improve the matching of the positive and negative current in order to avoid mismatch currents. Two additional transistors (T_{12}, T_{14}) are implemented. They assure that in case of switching the transistors T_{13} and T_{15}, their sources are already precharged, which reduces current peaks during the switching time.

B. Fully Programmable Multi-Modulus Divider

The divider is a fully programmable multi-modulus-divider, consisting of 7 asynchronously cascaded dual-modulus-2/3-dividers (Fig. 3). This assures that only the first stage runs at the high frequency of 2.4GHz. The divider is designed to convert the output signals of a

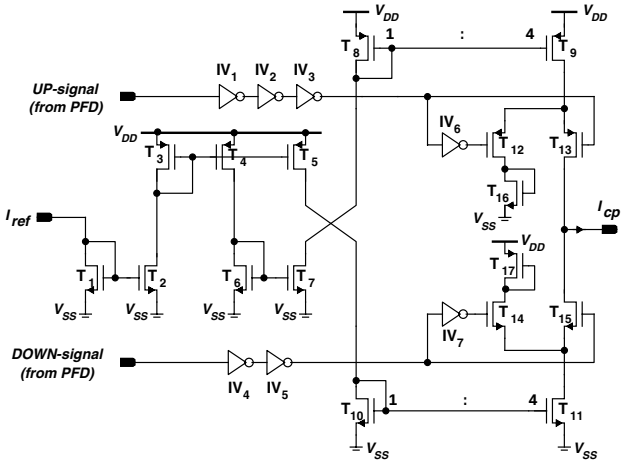

Fig. 2. Schematic of the tri-state-chargepump.

3rd-order MASH ΣΔ-modulator for a direct modulation of the PLL. The divider-value N can be programmed to all integer values in between 128 and 255, depending on the output bits $b_{0..6}$ of the ΣΔ-modulator: $N = 128 + \sum_{n=0}^{6} b_n \cdot 2^n$

This divider structure provides high flexibility and can also be used for other systems than Bluetooth. Practically, with a 3rd-order MASH ΣΔ-modulator only eight division-values are needed, but for test purposes in the prototype all values are accessible. Moreover, this divider structure does not need any additional logic such as a phase select state machine [1]-[2].

The simple logic of the AND/OR-gates assures that the modulus-signals of the last stages are produced first and given to the next stage. Thus the delay in the critical path – the feedback of the first divider-stage – is minimized. To reach operating frequencies of 2.5GHz, the first stages are realized in a differential source coupled logic (SCL). The tail currents in those stages are 100µA. The maximum

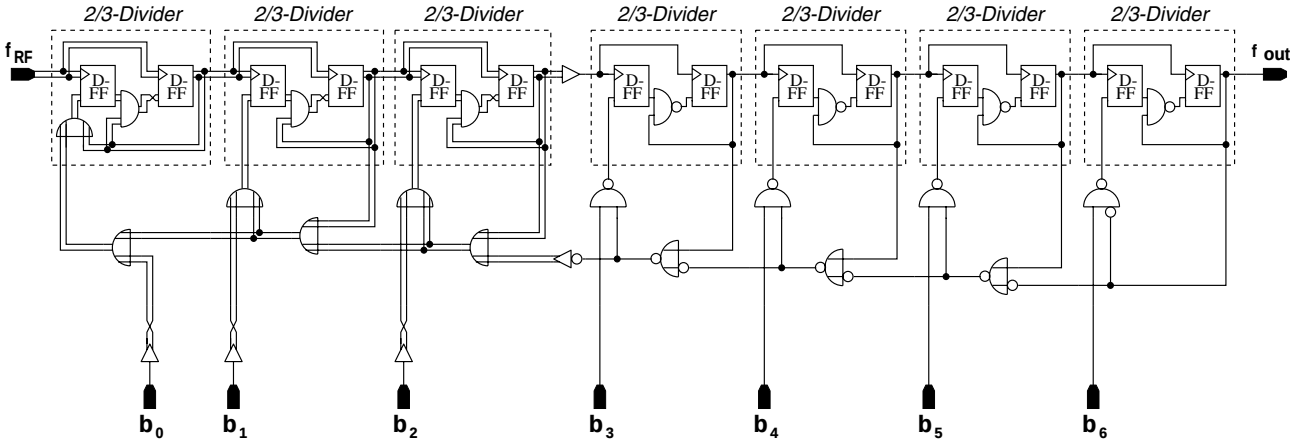

Fig. 3. Schematic of the fully programmable multi-modulus-divider.

operating speed is limited by the parasitic capacitance of the feedback of the first stage. Therefore a careful choice of the transistor sizes and a very accurate layout of the first stage are necessary to minimize the parasitic capacitance. To lower the current consumption, the following stages are realized with less power-hungry single-ended glitch-free true single phase clock (TSPC)-flipflops, which provide a maximum operating frequency of above 1 GHz [3].

The synchronization for the multi-modulus divider is necessary to assure that the output data of the 3rd-order ΣΔ-modulator are given to the divider at the right time and that no output data value will be missed or taken twice. It consists of two master-slave-D-flipflops per output bit. The first is clocked by the reference frequency and the second by the output signal of the divider.

C. Voltage Controlled Oscillator

The fully integrated VCO, shown in Fig. 4, contains a negative-Gm LC-Resonator with a cross-coupled pair of NMOS-transistors as active part. The LC-resonator is implemented as an on-chip spiral inductor and NMOS-varactors.

These varactors are realized by using the depletion region of the capacitance characteristic of the transistors. Beside the tuning input of the VCO an additional pair of NMOS-varactors are implemented as a second modulation input for the purpose of a two-point-modulation-PLL.

The RF output buffer is shown in Fig. 5. For testing purposes of the prototype, the RF output-buffer is used to measure directly the VCO-frequency with a spectrum analyzer. Due to the open-source structure of the buffer, an external balun can be used to convert the differential output of the VCO to a single-ended signal. If the buffer is not needed, it can be switched off by grounding the bias potential V_{bias4}.

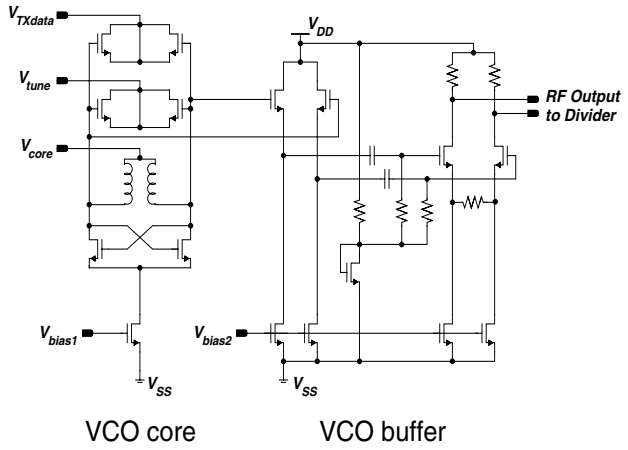

Fig. 4. Schematic of the fully integrated VCO.

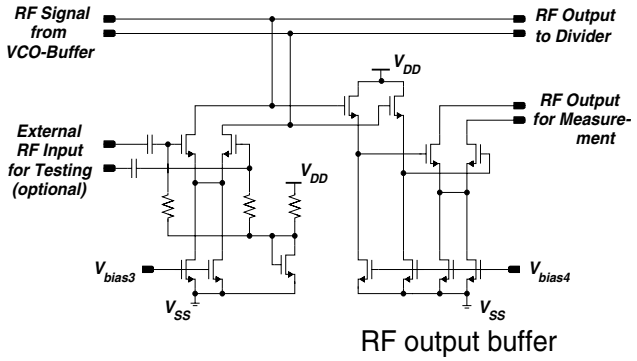

Fig. 5. Schematic of the RF output buffer.

III. Measurement Results

In the measurements the multi-modulus-divider reaches full functionality up to 2.41GHz. At higher frequencies the parasitic capacitance of the feedback in the first dual-modulus divider leads to malfunctions of the first stage. The modulus signals do not appear in time, therefore the divider is not working correctly beyond this frequency. The discrepancy between the simulations and measurements is caused by an insufficient model of the parasitic capacitance in the extractor tool. Further simulations show that the divider provides full functionality up to 2.7GHz by using an optimized layout. The total current consumption of the divider is about 6mA at 2.5V and can be further reduced by scaling down the current of the 2nd and 3rd stage.

Fig. 6 shows the VCO-characteristic. It is recognizable, that the measured tuning range of the VCO is slightly shifted down compared to the simulation. This is caused by the parasitic capacitance that is not exactly modeled in the extraction tool. In the next design step this will be taken into account in order to reach exactly the desired frequency range around 2.45GHz.

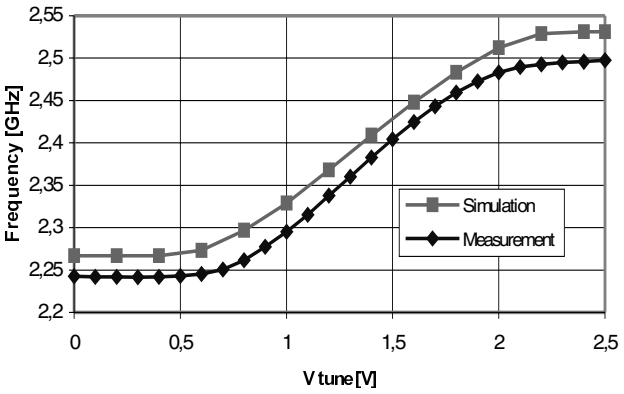

Fig. 6. VCO-Characteristics - Simulation vs. Measurement.

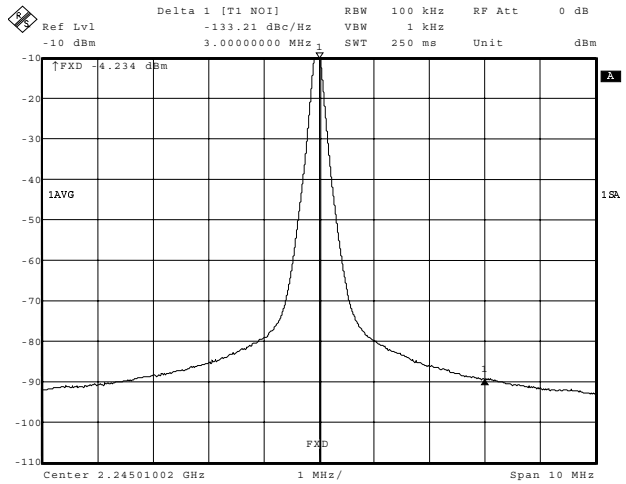

Fig. 7. Measured phase noise of the VCO.

While designing the VCO, a trade-off between power consumption, tuning sensitivity and tunable frequency range must be considered carefully. A decrease of the power consumption entails a decreased tunable frequency range and an increasing tuning sensitivity. The VCO in this frequency synthesizer provides a tuning sensitivity of about 200MHz/V, by consuming 1.5mA from a 2.5V supply. The tuning range spans from 2.24GHz to 2.5GHz. The VCO reaches a phase noise of -133dBc/Hz at 3MHz (Fig. 7).

The output spectrum of the frequency synthesizer in a locked state is shown in Fig. 8. At the distance of 13MHz the spurs of the reference frequency of about -68dBm are recognizable. Both the output spectrum and the phase noise meet the requirements of the Bluetooth specifications.

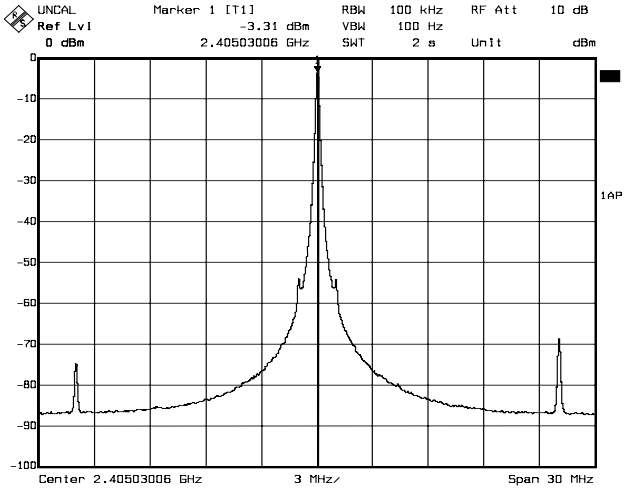

Fig. 8. Measured output-spectrum of the frequency synthesizer.

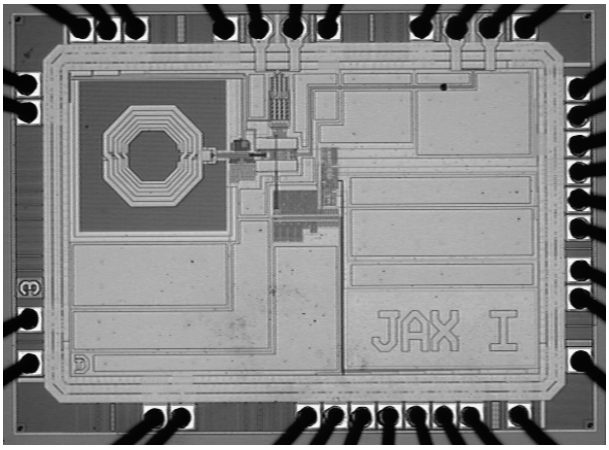

Fig. 9. Die photo of the frequency synthesizer.

As shown in the die photo of the chip (Fig. 9) the size of the prototype is particularly set by the pad frame, because of the large number of pads for testing purposes. In a further design step, the die size, which is currently 1.2 x 1.7 mm^2, can be reduced significantly. The integrated spiral inductor of the voltage controlled oscillator is recognizable in the upper left corner of the chip.

IV. Conclusion

A low power fully integrated 2.4GHz CMOS frequency synthesizer for the Bluetooth frequency range was presented. Compared to existing transmitter solutions in the frequency range for Bluetooth applications, the presented prototype provides a significant reduction of power consumption – one of the main goals for Bluetooth-solutions. Moreover, due to the fully integrated VCO the number of external components is reduced to a minimum, which reduces the production costs as well. The feasibility of the proposed structure is shown by measurements, and can be optimized by an improved layout.

References

[1] S. Willingham, M. Perrott, B. Setterberg, A. Grzegorek, B. McFarland, "An integrated 2.5GHz ΣΔ frequency synthesizer with 5 µs settling and 2Mb/s closed loop modulation," Proc. *IEEE International Solid State Circuits Conference 2000,* pp. 138-139, 2000.

[2] J. Craninckx, M. Steyaert, "A fully integrated CMOS DCS-frequency synthesizer," *IEEE Journal of Solid State Circuits,* vol.33, pp. 2054-2065, Dec. 1998.

[3] Q. Huang, R. Rogenmoser: "A glitch-free single-phase CMOS DFF for gigahertz applications," Proc. *IEEE International Symposium on Circuits and Systems 1994,* pp. 11-14, 1994.